

AO3401

30V P-Channel MOSFET

General Description

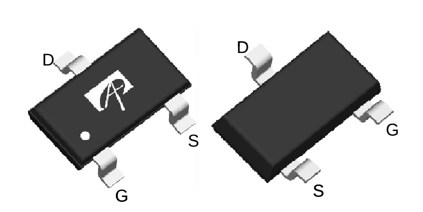
The AO3401 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

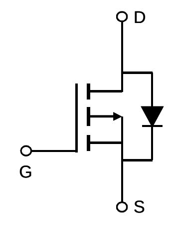
Product Summary

V_{DS}	-30V
I_D (at V_{GS}=-10V)	-4.0A
$R_{DS(ON)}$ (at V_{GS}=-10V)	< 50mΩ
$R_{DS(ON)}$ (at V_{GS} =-4.5V)	< 60mΩ
$R_{DS(ON)}$ (at V_{GS}=-2.5V)	< 85mΩ









Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25°C	I_D	-4	A
	T_A=70°C		-3.2	
Pulsed Drain Current [C]		I_{DM}	-27	
Power Dissipation [B]	T_A=25°C	P_D	1.4	W
	T_A=70°C		0.9	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	70	90	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		100	125	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	63	80	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	µA
		T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.5	-0.9	-1.3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=5V	-27			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-4.0A		41	50	mΩ
		T_J=125°C		62	75	
		V_{GS}=-4.5V, I_D=-3.7A		47	60	mΩ
		V_{GS}=-2.5V, I_D=-2A		60	85	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-4.0A		17		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
I_{SM}	Pulsed Body-Diode Current[B]				-27	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		645		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			55		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	4	7.8	12	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-4.0A		14		nC
Q_g(4.5V)	Total Gate Charge			7		nC
Q_{gs}	Gate Source Charge			1.5		nC
Q_{gd}	Gate Drain Charge			2.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=3.75Ω, R_{GEN}=3Ω		6.5		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			41		ns
t_f	Turn-Off Fall Time			9		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-4.0A, dI/dt=100A/µs		11		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-4.0A, dI/dt=100A/µs		3.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initialT_J=25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Fig 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

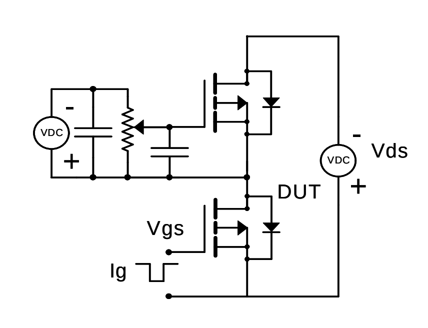
Figure 8: Capacitance Characteristics

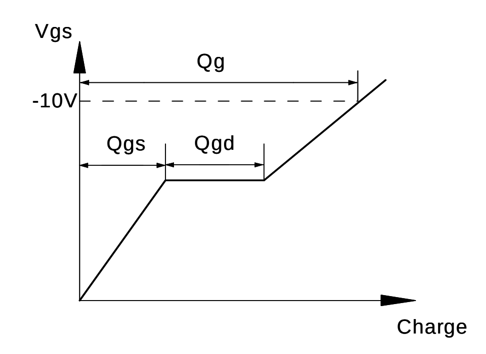
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

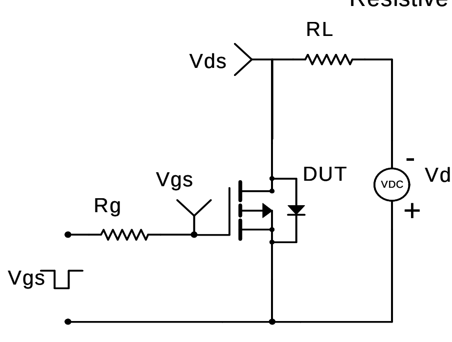
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

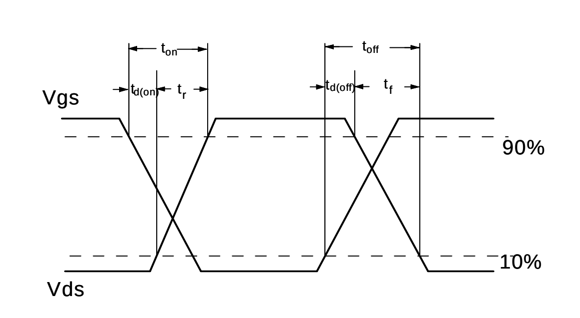
Gate Charge Test Circuit & Waveform



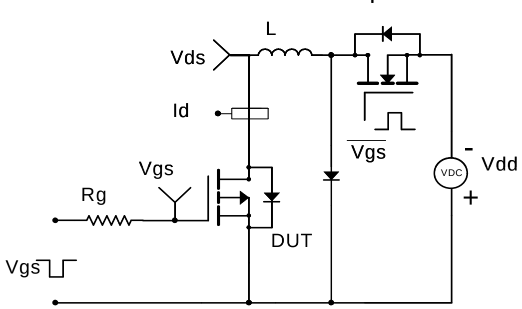


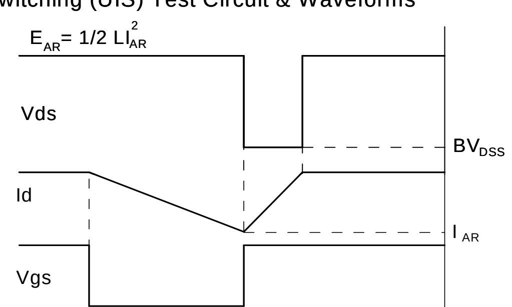
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms

